What is claimed is:

1.   A method comprising:

storing in memory a queue descriptor including a head pointer pointing to a first element in a queue and a tail pointer pointing to a last element in the queue;

in response to a command to perform an enqueue or dequeue operation with respect to the queue, fetching from the memory to a cache one of either the head pointer or tail pointer; and

returning to the memory from the cache portions of the queue descriptor modified by the operation.

2.   The method of claim 1 including fetching the head pointer and not the tail pointer in response to a command to perform a dequeue operation.

3.   The method of claim 1 including fetching the tail pointer and not the head pointer in response to a command to perform an enqueue operation.

4.   The method of claim 1 including returning to memory the head pointer and not the tail pointer if only dequeue operations were performed on the queue.

5.   The method of claim 1 including returning to memory the tail pointer and not the head pointer if only enqueue operations were performed on the queue while the queue was unempty.

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6.   The method of claim 1 including returning to memory the head pointer and tail pointer if an enqueue and a dequeue operation were performed on the queue, or an enqueue operation was performed on the queue while the queue was

10   empty.

7.   A method comprising:

determining whether a head pointer or a tail pointer of a queue descriptor that was fetched from memory to a cache

15   had been modified by an enqueue or a dequeue operation; and

returning a particular pointer to the memory from the cache only if that pointer had been modified.

8.   The method of claim 7 including using valid bits in the

20   cache to track modifications to the pointers.

9.   The method of claim 8 including using a first valid bit to track modifications to the head pointer and second valid bit to track modifications to the tail pointer.

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10. The method of claim 9 including setting the first valid bit if a dequeue operation is performed with respect to the queue descriptor, or an enqueue operation is performed with respect to the queue descriptor while the queue is empty.

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11. The method of claim 9 including setting the second valid bit if an enqueue operation is performed with respect to the queue descriptor.

10   12. The method of claim 9 including setting a pointer's valid bit when the pointer is fetched from the memory to the cache.

13. The method of claim 9 including returning to the memory

15   pointers whose valid bits have been set.

14. An apparatus comprising:

memory for storing queue descriptors which include a head pointer pointing to a first element in a queue and a

20   tail pointer pointing to a last element in the queue;

a cache for storing queue descriptors corresponding to up to a number of the memory's queue descriptors; and

a processor configured to:

fetch from the memory to the cache one of either

25   the head pointer or the tail pointer of a particular queue

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descriptor in response to a command to perform an enqueue or a dequeue operation with respect to the particular queue descriptor; and

return to the memory from the cache portions of

5   the queue descriptor modified by the operation.

15.   The apparatus of claim 14 wherein the processor is configured to fetch the head pointer and not the tail pointer in response to a command to perform a dequeue

10   operation.

16.   The apparatus of claim 14 wherein the processor is configured to fetch the tail pointer and not the head pointer in response to a command to perform an enqueue

15   operation.

17.   The apparatus of claim 14 wherein the processor is configured to return to the memory the head pointer and not the tail pointer when only dequeue operations were performed

20   on the queue.

18.   The apparatus of claim 14 wherein the processor is configured to return to the memory the tail pointer and not the head pointer if only enqueue operations were performed

25   on the queue while the queue was unempty.

19. The apparatus of claim 14 wherein the processor is configured to return to the memory the head pointer and tail pointer if an enqueue and a dequeue operation were performed

5   on the queue, or an enqueue operation was performed on the queue while the queue was empty.

20. The apparatus of claim 14 wherein the cache stores valid bots and wherein the processor is configured to track

10   modifications to the pointers in the cache by setting the valid bits.

21. The apparatus of claim 20 wherein the cache stores a first valid bit to track modifications to the head pointer

15   and a second valid bit to track modifications to the tail pointer.

22. The apparatus of claim 21 wherein the processor is configured to set the first valid bit if a dequeue operation

20   is performed with respect to the queue descriptor, or an enqueue operation is performed with respect to the queue descriptor while the queue is empty.

23. The apparatus of claim 21 wherein the processor is configured to set the second valid bit if an enqueue operation is performed with respect to the queue descriptor.

5   24. The apparatus of claim 21 wherein the processor is configured to set a pointer's valid bit when the pointer is fetched from the memory to the cache.

25. The apparatus of claim 21 wherein the processor is

10 configured to return to the memory the pointers whose valid bits has been set.

26. An article comprising a computer-readable medium that stores computer-executable instructions for causing a

15 computer system to:

store in memory a queue descriptor including a head pointer pointing to a first element in a queue and a tail pointer pointing to a last element in the queue;

in response to a command to perform an enqueue or

20 dequeue operation with respect to a queue, fetch from memory to a cache one of either a head pointer pointing to a first element in a queue or a tail pointer pointing to a last element in the queue; and

return to the memory from the cache the portions of the

25 queue descriptor modified by the operation.

27. The article of claim 26 including instructions to cause the computer system to:

fetch the head pointer and not the tail pointer in

5 response to a command to perform a dequeue operation; or

fetch the tail pointer and not the head pointer in

response to a command to perform an enqueue operation.

28. The article of claim 26 including instructions to cause

10 the computer system to return to memory:

the head pointer and not the tail pointer if only

dequeue operations are performed on the queue;

the tail pointer and not the head pointer if only

enqueue operations are performed on the queue while the

15 queue is unempty; or

both the head pointer and tail pointer if both an

enqueue and a dequeue are performed on the queue, or an

enqueue operation was performed on the queue while the queue

is empty.

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29. The article of claim 26 including instructions to cause

the computer system to set a valid bit corresponding to a

pointer in the cache when the pointer is modified by an

enqueue or a dequeue operation.

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30. The article of claim 29 including instructions to cause the computer system to return to the memory pointers whose corresponding valid bits are set.